REMARKS

Claims 1-18 are pending in this application of which claims 1, 5, 9, 13, and 14 are independent. Reconsideration of the rejected claims in light of the arguments presented below is respectfully solicited.

In response to the request for reconsideration of November 18, 2002, the Examiner now rejects claims 1-18 based on new prior art. Specifically, the Examiner rejects claims 1-18 under 35 USC § 103(a) as being unpatentable over Shimamoto, which was cited in the previous office actions, in view of Takahashi (US Patent Number 5,604,513). The rejection is respectfully traversed.

Regarding the Shimamoto reference, the Examiner reiterates the same reasoning as in the previous two office actions. Specifically, the Examiner relies on Shimamoto for teaching a liquid crystal display and display data transferred from a display timing circuit to a TFT liquid crystal panel. As previously explained, Shimamoto reduces electromagnetic interference, EMI, by transferring serial display signals at a low voltage and high speed from the display controller to the flat panel. A low voltage serial/parallel conversion circuit restores the low voltage signals, which are then supplied to the flat panel control circuit. Accordingly, the voltage conversions reduce the occurrence of EMI. The Examiner acknowledges that Shimamoto fails to teach the transfer of data in which display data lags one or another for each bit, however, relies on Takahashi to cope with the deficiencies of Shimamoto.

Takahashi discloses a serial sampling video signal driver which improves color rendition in color displays, *i.e.*, the video signal driver reduces the occurrence black and/or white dots blushed with color tinge. In order to reduce these effects, Takahashi teaches delaying green and blue analog video signals relative to the red analog video signal such that they are offset from

one another. In order to obtain a pure white dot or a pure black dot, the serial sampling video driver 10 samples each of the offset waveforms at the same point but at different times, as illustrated by Fig. 4. As compared to conventional techniques (Fig. 5), the analog video signals are sampled at different points along each waveform at the same time resulting in color tinge.

In general, EMI may be caused by simultaneously changing each data output signal of a multi-port system, which causes a high momentary generated current. This current may create electromagnetic noise, which negatively affects other system components. By delaying data output signals from one another, as embodied by the claims, only a small current is generated by each change thereby reducing the negative effects of EMI on other system components. EMI may be reduced in accordance with any one of the implementations recited by independent claims 1, 5, 9, and 13. Certain language of these claims have been reproduced below.

> Claim 1 recites, *inter alia*, "points of changing said data output signals with respect to a time base are set with time delays that lag one another during one period of a reference internal clock signal, so that number of simultaneous changes of display data output signals is reduced."
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> Claim 5 recites, *inter alia*, "points of changing said display data output signals with respect to a time base are set with time delays that lag one another during one period of a clock output signal or a reference internal clock signal having a same phase as the clock output signal, so that number of simultaneous changes of display data output signals is reduced."
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> Claim 9 recites, *inter alia*, "red, green and blue colored display data composed of plural bits are transferred ... each transfer is performed with a time delay that lags incrementally for each bit unit formed of plural bits optionally selected from each of said display data."
>
> Claim 13 recites, *inter alia*, "a display timing control circuit for transferring red, green and blue color display data formed of plural bits to the TFT drive circuit...; and a delay unit provided in the displayed timing control circuit to delay the transfer timing between one bit unit and another."

The Examiner alleges that the time delay feature common to independent claims 1, 4, 9, and 13 is disclosed by Takahashi. However, there is no motivation to combine Shimamoto and Takahashi, and further, the motivation to combine proposed by the Examiner is flawed.

The Examiner asserts that Takahashi teaches reducing EMI by delaying each data signal to lag from one another, and therefore, it would have been obvious to combine the references to reduce EMI. To the contrary, Applicants have fully reviewed the Takahashi reference, and find no suggestion of delaying data signals relative to one another for reducing EMI. In fact, contrary to the Examiner's allegations, Takahashi does not even address the occurrence of EMI. Instead, Takahashi addresses reducing the occurrence of color tinge by delaying analog data signals relative to one another and sampling each data signal along the same points of each waveform.

The Examiner's conclusion of obviousness (the reduction of EMI by delaying data signals) has been gleaned from the subject disclosure. That is, the examiner has based the conclusion of obviousness on an improper hindsight reasoning, which is contrary to legal precedence. Specifically, "[a]ny judgement on obviousness is in a sense necessarily a reconstruction based on hindsight reasoning, but so long as it takes into account only knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made and does not include knowledge gleaned only from applicants disclosure, such a reconstruction is proper." *In re McClaughlin,* 443 f.2d 1392 (CCPA 1971). The rejection should be withdrawn.

It is noted further that there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one in the ordinary skill in the art, to modify or combine the teachings. (See MPEP § 2143.01). The Federal Circuit has recently produced a number of decisions overturning obviousness rejections due to lack of a suggestion in the prior art of the desirability of combining references. The examiner has not

produced any teachings that delaying data signals relative to one another would reduce the occurrence of EMI, except for such teaching in the presence application.

In *arguendo*, assuming that motivation to combine could be established, the references are not combinable. In the simplest terms, Takahashi delays red, green, and blue analog signals and samples these signals along the same points in order to reduce color tinge in an analog environment. Shimamoto, the primary reference, does not even suffer from the effects of color tinge, as Shimamoto operates in the digital domain. Specifically, Shimamoto reduces electromagnetic interference, EMI, by transferring digital display signals at a low voltage and high speed from the display controller to the flat panel. A low voltage serial/parallel conversion circuit restores the digital low voltage signals, which are then supplied to the flat panel control circuit. Accordingly, the voltage conversions reduce the occurrence of EMI.

It would not be possible to modify Shimamoto with the teachings of Takahashi. Specifically, in Takahashi, the delay circuits are configured to delay red, green, and blue analog signals relative to one another. Sample and hold (S/H) circuits sample each analog waveform in accordance with a control signal, so that sampling is performed on the same point of each waveform. In order to modify Shimamoto with the teachings of Takahashi, one would have to incorporate circuitry configured for an analog environment in a display controller and apparatus (Shimamoto) operating in the digital domain. Such a combination is not possible and would not have been obvious.

For the above reasons, claims 1, 5, 9 and 13 and claims dependent therefrom are patentable as there is no motivation to combine Shimamoto with Takahashi as suggested by the Examiner. The Examiner has essentially taken two disparate references and alleged that they

teach the claimed invention. Such rationale is improper. Withdrawal of the rejection is respectfully solicited.

In consideration of claim 14, there are significant features of claim 14 which are neither disclosed by Shimamoto, Takahashi, or namely other things, "a detector circuit for detecting a coincidence of plurality by comparing a plurality of bits for each predetermined group of image data outputted by the data display circuit; a first control circuit ...; a second control circuit outputting data ... when the coincidence of plurality of bit has been detected by the detector circuit." Applicants have thoroughly reviewed Shimamoto and Takahashi and fail to find any disclosure or suggestion of the features of claim 14. Moreover, in the examiner's interview of November 13, 2002, an agreement was reach whereby the examiner admitted on the record that Shimamoto in view of Rindal did not teach "detecting coincidence of plurality of bits for each predetermined bit of image data output by the data supply circuit (claim 14)." However, in the present office action, the Examiner continues to argue that Shimamoto discloses the features of claims 14, some of which are recited above. With *emphasis added*, Shimamoto fails to teach the features of claim 14. The Examiner's assertions are even contrary to the Examiner's own admission on the record. The Examiner is urged to reconsider the claim 14 as Shimamoto and Takahashi do not even disclose or suggest in any manner detecting coincidence of plurality and outputting data when such coincidence of plurality has been detected, as claim 14 recites. Withdraw of the obviousness rejection is respectfully solicited.

In light of the remarks above, the obviousness rejection has been overcome. Applicants respectfully solicited prompt allowance of this case. If the Examiner has any questions regarding this response, or the application in general, the Examiner is requested to contact the undersigned.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

David M. Tennant
Registration No. 48,362

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 SAB:DT:men
Facsimile: (202) 756-8087
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